Remarks

Reconsideration and withdrawal of the outstanding rejections in consideration of this amendment is respectfully requested.

With the above-made amendments, claims 1-39 remain pending of which claims 1, 3-8, 10-11 and 19 are currently amended. (Claims 12-18 and 28-39 stand withdrawn as being directed to a non-elected invention.)

Amendments were made to the claims for purposes of effecting further clarification of the invention to be covered including in terms of more clearly defining the claims over the art documents as cited in the rejections. Additionally, with regard to independent claim 19, the preamble thereof, also, was revised to more appropriately conform to that set forth body of the claim.

With respect to independent claim 1, revisions were effected therein to more clearly define the vertical height relationships between the "first edge surface" and that of the "second edge surface" of the "embedding insulating film" embedded into the trench. This is explained with regard to Figs. 9 and 10 of the drawings in connection with the description of the formation of the embedding insulating film 103 (see Fig. 1D *et seq.*) and page 29 *et seq.* of the Specification, as well as the related discussion regarding stresses associated with the formation of the STI (Shallow Trench Isolation) region in conjunction with the impurity-caused stress associated with the formation of the ion implanted source and drain diffusion regions of the MOS transistors. Similar such clarifications, although somewhat differently presented from that in claim 1, were also implemented in other ones of the independent claims.

As can be seen from the plan view layout in Fig. 9 of the drawings, the element isolation trench 119 having the recessed edge surface, as seen by the stepped-down plane surface of embedding insulating film 103 in Fig. 10 of the drawings, is related to that element isolation region portion where the gate electrode is not positioned. As can be seen from the discussion related to Figs. 1E-1H, the well region 105 has ion implanted source and drain diffusion regions provided in correspondence to the gate electrode and that the "second edge surface" (see claim 1) or the "recessed plane within the trench" is positioned near the source and drain diffusion regions where the impurity concentration is greater than an impurity concentration of the well region. This can be seen from Figs. 9 and 10 as well as elsewhere in the drawings which show that at locations other than where the gate electrode is formed, the "embedding insulating film" in the trench has a boundary plane with, for example, the interlayer insulating film (e.g., oxide film 113 in Fig. 1F) that corresponds to a boundary plane at a vertically depressed position(i.e., a recessed plane) than that where the gate electrode is formed. As can be seen from Fig. 10 of the drawings, which is a sectional view corresponding to line B'-B of Fig. 9, the "first edge surface" according to claim 1 relates to an edge surface that is planar with the substrate surface while the "second edge surface" of the embedding insulating film in the trench relates to the depressed or recessed surface. Although somewhat differently presented due to use of modified language therein, similar such clarification was effected with regard to other ones of the above-noted independent claims.

Dependent claim 3 was also revised to remove some language that is,

basically, duplicative of language incorporated into base claim 1. In claims 4 and 5, the term "difference" was further clarified to relate to a height difference.

According to the outstanding Office Action, claims 1-8, 10-11 and 20 were rejected under 35 USC §102(b) as anticipated by Huang (USP 6,406,987); claim 19 was rejected under 35 USC §102(b) as anticipated by Tasaka (USP 5,561,078); claim 22 was rejected under 35 USC §102(e) as anticipated by Pividori(US 2003/010066 A1); claims 9 and 21 were rejected under 35 USC §103(a) as unpatentable over the combination of Huang, *supra*, and further in view of Nishioka (US 2002/0008019A1); and claims 23-27 were rejected under §103 as unpatentable over the combination of Pividori, *supra*, in view of Su (US 2002/0137282A1). It will be shown, hereinbelow, the invention according to these claims was neither disclosed nor would have been suggested in the manner as that alleged in the outstanding rejections. Therefore, insofar as presently applicable, these rejections are traversed and reconsideration and withdrawal of the same is respectfully requested.

Crystalline defects are sometimes caused in the element isolation region by the stress caused from the element isolation region (e.g., STI stress), the stress resulting from the implanted impurities in the active region such as in connection with the formation of the source and drain regions of a MOS transistor, *et seq*. For example, the growth of the oxide film on the side wall of the trench leads to volume expansion of, for example, silicon oxide (SiO_2) by the heat treatment after the element isolating insulating film is embedded in the STI trench. When silicon (Si) is changed into SiO_2, a volume expansion of SiO_2 may become two or more times

larger than the volume expansion of Si. Since such volume expansion is restrained by the presence of the embedded oxide film (e.g., 103), this causes even higher compression stresses (STI stresses) in the substrate which can lead to crystalline defects in the device, such as shown with regard to the discussion of Figs. 2-3 and 4-5.

Applicants schemed their invention to suppress such defects by avoiding added stresses. For example, consistent with the invention now set forth in claims 1+, 6-11, 19 and 20-27, the insulating film (e.g., embedding insulating film) in the STI trench is recessed, i.e., the upper edge surface of the insulating film is recessed to a level that is lower than the semiconductor substrate surface. Further, this recessing is effected near the relatively high concentration source and drain regions in the well of the active region. Due to a recessed surface of the embedding insulating film, the formation of crystalline defects can thereby be suppressed by reducing the restraints on the wall of the trench that is otherwise caused by the insulating film.

Such an aspect of the present invention which calls for the upper edge surface of the embedding insulating film to be recessed at a first element isolation region portion which is positioned synonymous with the edge surface of the trench (e.g., STI) near the heavily doped source and drain diffusion regions is in clear contradistinction with that disclosed by Huang. Huang, it is submitted, disclosed a process for recessing the element isolating insulating film for the STI in connection with forming the visor. Huang did disclose a scheme for forming reliable borderless contact openings to the silicon substrate extending over the active area/STI

interface. In this regard, Huang's scheme calls for the formation of "visors or protective coverings over the edge of the silicon active device areas to prevent electrical shorting of the diffused surface junctions to the substrate when borderless contacts are formed." (Column 3, lines 11-20, in Huang.) However, in Huang, when the contact such as 24 (corresponding to the electric plug; see Fig.10) is formed on the edge of the STI trench, for suppressing the short circuit due to the exposure of the trench side wall, which is caused by the over-etching at the edge of the STI, the exposed side wall of the trench is covered with the visor (20'). That is, in accordance with Huang's scheme, the exposed side wall of the trench is covered with the visor to suppress the short circuit between the source-drain diffusion region at the upper side of the side wall of the trench and the well region below the through-metal contact 24 and so forth. It is the short circuit that is caused on the side wall of the trench that is suppressed in accordance with Huang's scheme, unlike that according to the structural scheme presently called for in each of independent claims 1, 6, 7, 8, 10, 11, 20, *et seq.*

While Huang's disclosure features a process for recessing the element isolating insulating film for the STI in a formation of the visor (e.g., 20'), the invention as now called for sets forth a schemed semiconductor device in which the edge surface of the recessed insulating film (e.g., the "second edge surface" in independent claim 1) is positioned near where the concentration of the impurity is relatively largest in the active region such as with regard to the well region where the source and drain diffusion regions are formed, for example, the source and drain being ion implanted source and drain diffusion regions formed in

correspondence to the gate electrode. That is, in accordance with the present invention, the short circuit is not caused in the exposed portion of the trench in contradistinction with that according to Huang's scheme. It is submitted, Huang neither disclosed nor suggested a scheme calling for the insulating film deposited on the STI to be recessed such as for suppressing the crystalline defects caused by the stress of the trench, such as earlier explained in these remarks and, more extensively, discussed in the present Specification. Therefore, in view of at least the above reasons, the invention as now called for in claims 1-8, 10-11 and 20 could not have been anticipated nor, for that matter, realized in view of Huang's teachings.

The semiconductor device manufacturing scheme called for in claim 19, it is submitted, is also considered defining over Tasaka. The method according to claim 19 also features a scheme calling for the formation of a trench "which is embedded by an embedding insulating film" in such a way that the upper edge of the embedding insulating film in the trench is caused to become recessed from the surface of the active region at a position of the trench wall near the source and drain diffusion regions where impurity concentration is relatively large. It is submitted, a scheme which calls for such featured aspects was neither disclosed nor could have been realized in view of Tasaka.

The rejection makes reference to the discussion in column 1, lines 44+, in Tasaka regarding causing the embedding insulating film "to retreat from the surface of said active region ... ." However, as is now more clearly set forth in independent claim 19, the recessing of the embedding film according to the present

invention is a desirable and deliberate action in connection with avoiding defects associated with the STI and compression stress referred to earlier in these remarks and as explained in greater detail in the present Specification. Tasaka's scheme mentions the aspect of "over-etching" which occurs owing to "the difficulty in controlling the etching-back." Tasaka, neither disclosed nor suggested a semiconductor device manufacturing scheme which calls for forming the trench with the recessed "upper edge of the embedding insulating film" near the heavily doped source and drain regions, which are ion implanted source and drain diffusion regions provided in correspondence to the gate electrode. For at least the above reasons, the invention could not have been anticipated nor realizable in view of Tasaka.

The invention according to claims 22+ calls for a semiconductor device comprising a memory array constituted by memory cells arranged in a matrix on a semiconductor substrate and a peripheral circuit region where other circuit elements are formed. With regard to the invention according to claim 22, the device also calls for a plurality of element isolating portions made of an insulating film embedded into a trench on a major surface of this substrate. Further, the semiconductor device according to claim 22+ is characterized in that in the memory array, the recess amount of the element isolation portion is relatively large while in the peripheral circuit region, the recess amount of the element isolation portion is either at zero or at a relatively small amount. An example of this is given with regard to Fig. 21A of the drawings which is a sectional view along line A-A of Fig. 19 (which is a plan view of the major portion of the memory array in Fig. 17) and

Fig. 21B which is a sectional view of a major portion of a peripheral circuit region of the memory. As can be seen from Fig. 21A and Fig. 21B, the embedding insulating film in the STI is recessed at the location of the memory cells while it is substantially at a same plane as that of the substrate surface with regard to the peripheral circuit region as shown in Fig. 21B. The above can also be seen with regard to the embodiment shown in Fig. 42 of the drawings. It is submitted, such a scheme as that called for in independent claim 22 and as further according to the corresponding dependent claims 23-27 thereof could not have been anticipated nor realizable from Pividori even if combined with Su.

Pividori discloses only that since the CMP (Chemical-Mechanical Polishing) is performed more effectively in the center than along the outside, a recess condition or a protrusion condition of the insulating film differs between that of the center location to that near the edges of the trenches. That is, Pividori discloses that when etching is performed on the basis of the protruded portion, the recess amount of the STI insulating film is changed. It is submitted, Pividori neither disclosed nor suggested the featured aspects called for in claim 22, for example, that the recess quantity of the STI insulating film is changed in accordance with the width of the active region(see claim 23). In addition, Pividori neither disclosed nor suggested effecting different recess quantities between that associated with the STI's of the memory cell array and that associated with elements of the peripheral circuitry(see claim 24).

Su discloses STI (e.g., 11) in connection with a flash memory scheme. Su, however, neither disclosed nor appeared to suggest effecting/changing the recess amount associated with the embedding insulating film in the trench in accordance with the width of the active region. In fact, Su did not appear to be concerned with

the aspect of effecting a recess in the STI. It is submitted, therefore, Su also cannot attain the effect of the present invention, for example, suppressing the concentration of the stress in the substrate.

The present inventors realized that the compression stress is distributed concentrically on the region where the width of the active region is relatively narrow and the pattern density is high. Accordingly, applicants have schemed their invention such that the recess quantity is changed in accordance with the width of the active region to suppress the generation of the crystalline defects, referred to earlier in these remarks.

Tasaka neither disclosed nor suggested the formation of an embedding insulation film in a trench with a recessed surface in a manner as that presently called for. Nishioka also does not overcome the deficiency in Huang. Nishioka, it is submitted, failed to disclose or suggest changing a recess quantity of the embedding insulating film of the trench in connection with achieving a semiconductor device avoiding the defect concerns addressed earlier in the remarks and thereby achieve excellent performance. It is submitted, therefore, the invention according to claims 9 and 21, as combined with claims 1 and 20, respectively, could not have been achievable over the combined teachings of Huang and Nishioka.

For at least the above reasons, the invention according to claims 1-11 and 19-27 could not have been realizable in a manner as that alleged in the outstanding rejections. Therefore, in view of the amendments presented hereinabove together with these accompanying remarks, reconsideration and withdrawal of the outstanding rejections as well as favorable action therefor on

these claims and an early formal Notification of Allowability is respectfully requested.

To the extent necessary, applicants petition for an extension of time under 37 CFR §1.136. Please charge any shortage in the fees due in connection with the filing of this paper, including Extension of Time fees, to the Deposit Account of Antonelli, Terry, Stout & Kraus, LLP, Dep. Acct. No. 01-2135 (500.42877X00), and please credit any excess fees to such deposit account.

Respectfully submitted,
ANTONELLI, TERRY, STOUT & KRAUS, LLP

Larry N. Anagnos
Reg. No. 32,392

LNA/dks
703-312-6600